AD-A216 180

# REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188



1. AGENCY USE ONLY (Leave blank)

2. REPORT DATE: February 6, 1982

3. REPORT TYPE AND DATES COVERED: Final (May 1, 1980-May 31, 1981

4. TITLE AND SUBTITLE: FAULT TOLERANT VLSI DESIGN ASSESSMENTS FOR ADVANCED AVIONICS DEPARTMENT

5. FUNDING NUMBERS: 61102F 2306/B2

6. AUTHOR(S):
Satinderpaul S. Devgan and
Mr. Robert A. Alexander

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES):
Tennessee State University
Department of Electrical Engineering
3500 Centennial Blvd
Nashville, Tennessee 37203

8. PERFORMING ORGANIZATION REPORT NUMBER: AFOSR-TR- 89-1631

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES):
AFOSR
BLDG 410
BAFB DC 20332-6448

DTIC ELECTE DEC 06 1989 S B D

10. SPONSORING/MONITORING AGENCY REPORT NUMBER: F49620-80-C-0089

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

With the advances in VLSI technology, it will be possible to fabricate chips with 100,000 to 500,000 gates per chip. Rather the technology to pack more and more elements on a chip has outpaced the collective knowledge for effective use of chip "real estate". For example, it is virtually impossible to test high density microcircuits. This report reviews the existing literature on VLSI technology with regards to proposed methods to increase reliablity and testablilty. One of the cristical problems of high density microcircuits is the limited number of I/O pins. The proesent literature points out the two types of circuilt additions that can improve circuit reliability. The reprot also provides a list of refereces for further study of Fault-Tolerant Computing.

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

14. SUBJECT TERMS

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT: unclassified

18. SECURITY CLASSIFICATION OF THIS PAGE: unclassified

19. SECURITY CLASSIFICATION OF ABSTRACT

20. LIMITATION OF ABSTRACT

NSN 7540-01-280-5500

Standard Form 298 (890104 Draft)
Prescribed by ANSI Std. 239-18
298-01

AFOSR-TR- 89-1831

# FAULT-TOLERANT VLSI DESIGN ASSESSMENTS FOR ADVANCED AVIONICS DEPARTMENT

Literature Review

Satinderpaul S. Devgan and Robert A. Alexander
Department of Electrical Engineering
Tennessee State University
3500 Centennial Blvd.
Nashville, Tennessee 37203

February 5, 1982

Final Report for:

Distrubution of this document is unlimited

Prepared for:

AIR FORCE OFFICE OF SCIENTIFIC RESEARCH
Bolling Air Force Base,
Washington, DC 20332

AIR FORCE AVIONICS LABORATORY
Wright Patterson Air Force Base, Ohio 45433

89 12 05 170

## ABSTRACT

With the advances in VLSI technology, it will be possible to fabricate chips with 100,000 to 500,000 gates per chip. Rather the technology to pack more and more elements on a chip has outpaced the collective knowledge for effective use of chip "real estate". For example, it is virtually impossible to test high density microcircuits.

This report reviews the existing literature on VLSI technology with regards to proposed methods to increase reliability and testability. One of the critical problems of high density microcircuits is the limited number of I/O pins. The present literature points out the two types of circuit additions that can improve circuit reliability.

The report also provides a list of references for further study of Fault-Tolerant Computing.

## FOREWORD

The research reported here was performed by the Department of Electrical Engineering, under contract #F49660-80C-0089. Ms. Joan Marshall was the contracting officer for the Air Force Office of Scientific Research. Mr. Robert Alexander was the Principal Investigator for the Department of Electrical Engineering at Tennessee State University in Nashville, Tn. The authors appreciate the assistance provide by Ms. Marshall and the Air Force office of Scientific Research for funding the project. Also, the authors would like to acknowledge the support and guidance provided by Lt. Col. Gardner and retired Lt. Col. Eugene Jones.

## TABLE OF CONTENTS

## INTRODUCTION

Contemporary integrated circuits contain as many components as the largest computing systems of 15 to 20 years ago. [1] The 1960's were the decade of gate level design, the 1970's were the decade of register-transfer-level design and the 1980's will be the decade of processor-memory switch (PMS) design. The age of VLSI is here and its technology is presenting interesting potentials as well as challenges. The advantages of VLSI include reduction in support cost, improved reliability and improved fault detection. Some of the challenging issues include partitioning, fault models and dependencies, efficient use of redundancy, role of reliability tools, hierarchical complexity, self-test during operation, redundancy to enhance yield, and self-test at fabrication time.

As is the case in most design efforts, three primary factors were considered and traded off against each other in the design of computer systems: cost, performance and fault tolerance. In the past, systems engineers had realized that any attempt to improve significantly any one of these factors while holding another constant meant significant degradation in the third factor. [2] The advent of VLSI however, seems to have affected that situation dramatically. With VLSI, the economics are different and the rate of increase in cost as a function of added gates is greatly reduced. Thus, if a system designer wants to increase fault tolerance by adding circuitry while holding performance constant (or perhaps even increasing performance) the net increase in manufacturing cost of the machine will be very small in comparison to

costs for conventional designs of the past. [2] As the era of VLSI and VHSI circuits emerges, one integral chip will impart electronic functions of former systems. This factor tends to improve physical design economics, improve performance and on the surface, improve reliability and system availability. But problems of initial yield in chip fabrication such as increased complexity, cost of testing, etc, dramatically erode the economic advantages of increased circuit densities. In particular, the technology to pack more and more active elements on a chip has outpaced the collective knowledge for systematic and effective use of chip "real estate". For example it is virtually impossible to test high density micro-circuits in the laboratory and certainly not in their operational evironment.

The phase I of this research is to review literature and investigate the technological and economic feasibility of functional sub-circuit partitioning which elevates redundancy to the sub-circuit level (and beyond) to include higher levels of fault detection and fault isolation capability on a single chip. The purpose of the literature review is to ferret out key factors relevant to the design stage of electronic circuitry that dominantly affect end-user utility in the positive and negative sense. Another facet of the literature review is to acquaint the researchers with the immense literature base for electronic technology applicable to military avionics.

## LITERATURE REVIEW

In the past, the design of fault-tolerant computing systems has been done in an ad hoc manner. The absence of a unified theory of fault-tolerant computing can be attributed to at least two factors:

1. The high cost of hardware which in the past has limited the use of redundancy techniques.
2. A lack of understanding of the basic definitions and goals of fault-tolerant computing.

Avizienis [3] defined a fault-tolerant computer as one which is free from hardware and software design faults and can execute its programs correctly, obtaining correct results within specified time limits, despite the presence of transient or permanent operational faults.

The first special issue on Fault Tolerant Computing was published in the IEEE Transactions on Computers nearly a decade ago. [4] Six other special issues devoted to this same topic (5,6,7,8,9,10) contain a respresentative sample of the research activities that have taken place in fault-tolerant computing over the past decade.

The most obvious trend is the increasing concern with the effects of large scale integration on fault-tolerance techniques that were effective for computers implemented with SSI or MSI circuits. Different failure modes may be anticipated as the scale of integration increases; testing and diagnostic procedures that were appropriate ten years ago may be totally inadequate for the much more highly integrated circuitry of today.

Fault-tolerance has now come to be recognized as a desirable and in some cases an essential feature of a wide range of computing systems.

Interest in computers capable of long maintenance free operation has been matched by interest in low maintenance or scheduled maintenance commercial systems; inflight-control avionic systems that provide extremely high availability, process control and telephone switching systems. Also the fact that as more and more memory cells are packed into a single chip, the number of failure modes increases and the need for efficient algorithms to detect faults in them becomes more critical.

The formulation of the concepts of self checking logic[11] and hybrid redundancy[12] appear to be two important steps toward a general theory of fault-tolerant computing. Hybrid redundancy bridges the gap between static and dynamic redundancy schemes[13] while self checking design enables us to distribute the monitoring function among the sub-systems. Sedmak and Liebergol,[14] in describing a design approach for fault-tolerant general purpose computers implemented with VLSI, noted that there are significant problems in using some conventional fault-tolerant techniques in VLSI implementations. Their approach is to implement all the logic needed to detect faults in a VLSI chip directly on the chip itself and to design and partition this logic so as to minimize the possibility that any failure mode is capable both of causing a chip to malfunction and of simultaneously making it capable of reporting this fact.

## Fault-Tolerant Aspects

These are several parameters which affect the design of the fault-tolerant features as follows:

a. Nearly 100 percent immediate fault detection is necessary.

b. Complete recovery should be effected from transcient or intermediate failures.

:. Rapid fault-isolation, without human intervention will result in low down time.

The fault-tolerant aspects of the VLSI circuits are fault detection, isolation and recovery. By the mid 1980's it is expected that speeds for military avionics circuits will approach $10^8$ operations per second and the density of circuits will increase and the testing methods will become expensive and complex if not impossible. Since circuit densities in the range of $10^5$ to $5 \times 10^5$ gates per chip are within the reach of VLSI technologies today,[1] testability and reliability will become dominant issues. There is a large amount of literature on fault-tolerant computing, beginning with Von Neumann[15] and Moore and Shannon.[16] Of the recent literature on fault-tolerant computing, a large number of papers have focused on fault-tolerant memory. Reviews of semiconductor memory have been given by Eimbinder,[17] Riley [18] and Lenke et al.[19]

Several important past studies are pertinent to the background of this research. Agarwal addresses the problem of detecting faults in programmable logic arrays (PLA's). He points out that such devices are vulnerable to a unique class of contact faults and he develops a PLA model where in these faults can be represented. Crouzet and Laudrault contend that an LSI circuit can be made self-checking if it is designed from the out-set with that goal in mind and if its various possible failure modes are well understood. [10] Satish Thatte of TTI proposes several methods for improving VLSI testability. He proposes to utilize self-checking, on chip testing, partitioning and exhaustive checking and micro diagnostics.[1]

Lee, Ghani and Heron[20] suggest the use of recovery cache to take care of faults due to software. The function of a cache is to store all data that would be needed to restore a machine to the state it was prior to the execution of any defective software module.

A large amount of recent work has dealt with reconfiguration (manual and automatic) to improve system performance. Mathur and de Sousa [21] presented a technique which uses configurable NMR. Papers by Cox and Carroll[22] and Hartwell et al.[23] describe approaches which involve swapping memory bit planes. Srinivasan's[24] approach combines triple-modular redundancy (TRM) with matching the address decoder to the particular faulty array. Mehta et al [25] also addressed the issue of internal redundance while Carter and Schneider[12] discussed the basic principles of self-checking circuits.

Arnold[26] showed the importance of having fault detection and recovery for all the elements of a machine in order to achieve high reliability. Tanaka et al[27] described the use of duplication in some parts of a general purpose computer.

## SUMMARY


The critical problem with the VLSI circuits is the limited number of I/O pins. As the number of functions that can be done has increased, the pin outs have remained basically the same. This presents problems in that the chips have to be partitioned to make use of the limited I/O pins. Likewise, the interconnection between chips has become more difficult because of limited I/O pins.

Since "soft faults" can no longer be isolated by "hard fault" error detection devices, self-testing methods must be used to improve diagnostics and testing must move into the design level. As systems are currently partitioned into sub-systems, so can VLSI chips be partitioned into subcircuits. Critical subcircuits may be duplicated to provide redundant paths automatically after errors are detected. The device density gain will be traded off for circuit reliability as we try to pack more and more elements on chips. It is also envisioned that some redundant circuits will be provided to allow testability since high density circuits make it impossible to test circuits in the laboratory and in the field.

Following are the main methods used to increase reliability and testability. The first method is called fault masking. This is a process of masking a fault without really knowing the nature or location of the fault. Triple modular redundancy (TMR) and two rail networks (TRN) are techniques used in fault masking. These designs have a high redundant ratio i.e. ratio of hardware in redundant circuits to that of a nonredundant circuit is 3:1 to 4:1. The second method called self-checking is a process which detects possible error conditions in the circuit and produces an error signal which can be used to (1) stop

computations, (2) signal manual repair and (3) initiate reconfiguration of the circuit operation. The simplest form of this is complete duplication. The redundancy ratio of this type of circuit is greater than 2:1. Another type of self-checking circuit used forced-parity which involves adding additional hardware to the checking circuit which possesses the ability to generate an odd parity error.

Another design technique that is being extensively used by IBM is called the Level-Sense Scan Design (LSSD). The basic premise of this technique is that no feedback loops can be used in the chip. All loops must be broken down and replaced by serial shift registers/latches. The latches are then brought out to pins, there by allowing access to previously unreachable nodes within the chip thus having the shift register pin will also allow a test pattern to be entered into the chip register. From the work done so far, it is apparent that additional searching of the leterature is necessary. A bibliography at the end of the report offers additional helpful material that has not yet been studied by the researchers. This list will include additional literature that is being generated on this topic by various research organizations.

Equipment

A Motorola M6809 Development System was purchased under the Phase I of the project. This development system will be used to conduct tests on chip reliability and testability of various proposed designs. This equipment will also be used to train graduate engineers who will become well versed in VLSI/VHSI principles that will include considerations of economics, scale, speed and circuit utility.

## REFERENCES


1. D. Siewiorek and D. Rennels, "Fault-Tolerant VLSI Design", Workshop Report, IEEE Computer Journel, Dec. 1980, pp. 51-53.

2. R. M. Sedmak and H. L. Liebergol, "Fault-Tolerance of a General Purpose Computer Implemented by Very Large Scale Integration", IEEE Trans. on Computers, vol. C-29, No. 6, June 1980, pp 492-500.

3. A. Avizienis, "The Methodology of Fault-Tolerant Computing", Proc. of the First U.S.A. - Japan Computer Conference, Tokyo, Oct. 1972, pp. 405-413.

4. J. J. Stiffler, Guest Editor, "Special Issue on Fault-Tolerant Computing" IEEE Trans. on Computers, vol. C-20, Nov. 1971.

5. "Special Issue on Fault-Tolerant Computing", IEEE Trans. on Computers, vol. 22, March 1973.

6. "Special Issue on Fault-Tolerant Computing", IEEE Trans. on Computers, vol. 23, July 1974.

7. "Special Issue on Fault-Tolerant Computing", IEEE Trans. on Computers, vol. 24, May 1975.

8. "Special Issue on Fault-Tolerant Computing", IEEE Trans. on Computers, vol. 25, June 1976.

9. "Special Issue on Fault-Tolerant Computing", IEEE Trans. on Computers, vol. 26, June 1978.

10. "Special Issue on Fault-Tolerant Computing", IEEE Trans. on Computers, vol. 29, No. 6, June 1980.

11. F. P. Mathur and A. Avizienis, "Reliability Analysis and Architecture of a Hybrid-Redundant Digital System: Generalized Triple Modular Redundancy with Self-Repair", AFIPS Conf. Proceedings, vol. 36, (1970 Spring Joint Computer Conference) AFIPS Press. pp. 375-383.

12. W. Carter and P. Schneider, "Design of Dynamically Checked Computers" in Proc IFIP 68, Aug. 1968, pp. 878-883.

13. R. A. Short, "The Attachment of Reliable Digital System Through the use of Redundancy - A Survey", IEEE Computer Group News, vol. 2, No. 2, pp. 2-17, March, 1968.

14. R. M. Sedmak and H. L. Liebergol, "Fault-Tolerance of a General Purpose Computer Implemented by Very Large Scale Integration", IEEE Trans. on Computers, vol. C-29, No. 6, June 1980, pp. 492-500.

15. J. Von Neumann, "1952 Lectures , in Automate Studies, C.E. Shannon and J. McCarthy Eds. Princeton, N.J., Princeton University Press, 1956 pp 43-98.

16. F. H. Moore and C. E. Shannon, "Reliable Circuits Using Reliable Relays", J. Franklin Inst., Vol. 262, pp 191-208.

17. Semiconductor Memories , J. Eimbinder, John Wiley, New York 1971.

18. W. B. Riley, "Special Report: Semiconductor Memories are Tested Over Data-Storage Application", Electronics, vol. 46, August

19. G. Luecke, J. P. Mize and W. N. Carr, Semiconductor Memories, Design and Application , New York, McGraw Hill, 1973.

20. P. A. Lee, N. Ghani and K. Heron, "A Recovery Cache for the PDP-11" Digest of Papers, The Ninth Annual International Symposium on Fault-Tolerant Computing, Madison, Wise, pp 3-8, June 1979.

21. F. P. Mathur and P. T. de Sousa, "Reliability Models of NMR Systems", IEEE Trans. Rel. vol. R-24, pp 108-113, June 1975.

22. G. W. Cox and B. D. Carroll, "Reliability Modeling and Analysis of Fault-Tolerant Memories", IEEE Trans. Rel. vol. R-27, pp 49-54, April, 1978.

23. W. T. Hartwell, C. W. Hoffner and W. N. Toy, "A Fault-Tolerant Memory for Duplex Systems", IEEE Trans. Rel. vol. R-27, pp 134-138, June, 1978.

24. C. V. Srinivasan, "Codes for Error Correction in High Speed Memory Systems", Part I: Correction of Cell Defects in Integrated Memories", IEEE Trans. Computers, vol. C-20, pp 882-888, August 1971.

25. M. A. Mehta, et al., "Functions for Improving Diagnostic Resolution in an LSI Environment", in Spring Joint Computing Conf. AFIPS Conf. Rec. 1972.

26. J. F. Arnold, "The Concept of Coverage and its Effects on the Reliability Model of a Repairable System", IEEE Trans. Computing vol. C-22, pp 251-255, March 1973.

27. N. Tanaka, et al. "Computer with Designed in Duplication at Device Module Level", Tokyo Nikkei Electronics, March 1977.

BIBLIOGRAPHY

W. C. Carter and C. E. McCarthy, "Implementation of an Experimental Fault-Tolerant Memory System", IEEE Trans. on Computers, vol. C-25, No. 6, June 1976, pp. 557-568.

J. Losq, "A Highly Efficient Redundancy Scheme: Self-Purging Redundancy", IEEE Trans. on Computers, vol. C-25, N. 6, June 1976, pp. 569-578.

H. Y. H. Chuang, "Fail-Safe Asynchronous Machines with Multiple Input Changes", IEEE Trans. on Computers, vol. C-25, No. 6, June 1976, pp. 637-642.

R. C. Aubusson and I. Catt, "Wafer-Scale Integration- A Fault-Tolerant Procedure", Journal of Solid-State Circuits, vol. SC-13, No. 3, June 1978, pp. 339-344.

D. A. Anderson, "Design of Self-Checking Digital Networks Using Coding Technique", University of Illinois Coodinated Conf. AFIPS Conf. Rec. 1972.

C. Mead and L. Conway, "Introduction to VLSI Systems" Addison Wesley Publishing Co., 1980.

B. M. Chazelle and L. M. Monier, "Towards More Realistic Models of Computation for VLSI", Proc. of Cal Tech Conference on VLSI, Jan. 1981.

B. M. Chazelle and L. M. Monier, "Optimality in VLSI", Report prepared by the Department of Computer Science, Carnigie-Mellon University, Pittsburg, Pa, Sept. 1981, pp. 1-11, Tech. Report #CMU-CS-81-141.

D. P. Siewiorek, M. Canepa and S. Clark, "The Architecture and Implementation of a Fault-Tolerant Multiprocessor", Proceedings of the Seventh Annual International Symposium on Fault-Tolerant Computing, IEEE Computer Society, 1977 pp. 37-43.

A. Avizienis, "Fault-Tolerant Computing: An Overview", IEEE Trans. on Computers, vol. 4, pp. 5-8, Jan-Feb. 1971.

R. Teoste, "Design of a Repairable Redundant Computer", IRE Trans. Electron, Computing, vol. EC-11, pp. 643-649, Oct. 1962.

J. A. Abraham and D. P. Siewiorek, "An Algorithm for the accurate Reliability Evaluation of Triple Modular Redundancy Networks", IEEE Trans. on Computers, vol. C-23, pp. 682-692, July, 1974.

W. C. Carter, K. A. Duke and D. C. Jessep, "A Simple Self-Testing Decoder Checking Circuit", IEEE Trans. on Computers, vol. C-20, No. 11, pp. 1413-1414, November 1971.

Bibliography cont.


B. Parhami, "Techniques for the Design and Evaluation of Self-Checking Systems", Report Submitted to the Mathematical and Information Science Division of the Office of Naval Research, Arlington, VA, under contract #N00014-72-C-0459, February 1974.

D. R. Schertz, "Fault-Tolerant Computing: An Introduction", IEEE Trans. on Computers, vol. C-23, No. 7, July 1974.

W. C. Carter, "Fault-Tolerant Computing: An Introduction and a Viewpoint", IEEE Trans. on Computers, vol. 63, pp 225-229, March 1979.

J. F. Meyer and R. J. Sundstrom, "On Line Diagnosis of Unrestricted Faults", IEEE Trans. on Computers, vol. C-24, No. 5, May 1975.

F. J. O. Dias, "Fault Masking in Combinational Logic Circuits", IEEE Trans. on Computers, vol. C-24, No. 5, May 1975, pp 476-482.

A. L. Hopkins, Jr. and T. B. Smith, III, "The Architectural Element of a Symmetric Fault-Tolerant Multiprocessor", this issue IEEE Trans. on Computers, vol. C-24, No. 5, May 1975, pp 498-505.

C. R. Kime, "Fault-Tolerant Computing: An Introduction and a Perspective", IEEE Trans. on Computers, vol. 24, C-5, May 1975.

W. G. Bouricius, W. C. Carter, K. A. Duke, J.P. Roth and P. R. Schneider, "Interactive Design of Self-Testing Circuitry", Proceedings of the Purdue Centennial Year Symposium on Information Processing, Lafayette, Indiana, April 1969, pp 73-80.

W. C. Carter, D. C. Jessep, W. G. Bouricius, A. B. Wadia, C. E. McCarthy and F. G. Milligan, "Design Techniques for Modular Architecture for Reliable Computer Systems:, IBM Thomas J. Watson Research Center, Yorktown Heights, N. Y., Report RA-12, March 1970.

W. C. Carter, W. G. Bourieius, D. C. Jessep, J. P. Roth, P. R. Schneider and A. B. Wadia, "A Theory of Design of Fault-Tolerant Computers Using Standby Sparing", Digest of the International Symposium on Fault-Tolerant Computing, Pasadena, CA, March 1971, pp 83-86

J. F. Wakerly, "Partially Self-Checking Circuits and Their Use in Performing Logical Operations", Digest of the Interntional Symposium of Fault-Tolerant Computing,

D. A. Anderson and G. Metze "Design of Totally Self-Checking Check Circuits for m-out-of-n Codes", IEEE Trans. on Computers, vol. C-22, No. 3, pp 263-269, March 1973.

Special Issue, "Fault-Tolerant Computing: An Introduction", IEEE Trans. on Computers, vol. C-25, No. 6, pp 553-555, June 1976.

Bibliography cont.

R. C. Aubusson and I. Catt, "Wafer Scale Integration - A Fault-Tolerant Procedure", Journal of Solid-State Circuits, vol. SC-13 , No. 3, pp. 339-344, June 1978.

R. P. Capece, "Tackling the Very Large-Scale Problems of VLSI: A Special Report", Electronics, pp. 111-125, November 23, 1978.

E. A. Torrero, "VLSI and Other Solid-State Devices", Technology, IEEE Spectrum, vol. 16, No. 3, May 1979.

R. N. Gossen Jr., "1000,000 + Gates on a Chip: Mastering the Minutia", IEEE Spectrum, vol. 16, No. 3, pp. 42-47, March 1979.

W. M. Van Cleemput, "Hierarchical Design for VLSI: Problems and Advantages", Technical Note NO. 150, Computer Systems Laboratory, Dept. of Electrical Engineering and Computer Science, Stanford University, Contract #N-00014-75-C-0601, March 1979, pp. 1-16.

R. M. Davis, "The DOD Initiative in Integrated Circuits", IEEE Computer, pp. 74-79, 1979.

R. A. Cliff, "Acceptable Testing ofVLSI Components which Contain Error Correctors", IEEE Journal of Solid State Circuits, vol. SC-15, No. 1, pp. 61-70, February 1980.

J. H. Wensley, K. N. Levitt, M. W. Green, J. Goldberg and P. G. Neumann, "Design of a Fault-Tolerant Airborne Digital Computer Volumne I Architecture", Stanford Res. Inst. Melno Park, CA, Final Report, October 1973.

P. G. Neumann, K. N. Levitt, J. Goldberg and J. H. Wensley, "A Study of Fault-Tolerant Computing", Stanford Res. Inst. Melno Park, CA, Final Report Contr. #N0014-72-C-0254.

F. P. Mathur and P. T. de Sousa, "Reliability Models of NMR Systems", IEEE Trans. Rel. vol. R-24, pp.108-113, June 1975.

G. W. Cox and B. D. Carroll, "Reliability Modeling and Analysis of Fault-Tolerant Memories", IEEE Trans. Rel. vol. R-27, pp. 49-54, April 1978.

R. P. Cenker, et al, "A Fault-Tolerant 64K Dynamic Random-Access Memory", IEEE Trans. Electron Devices, vol. Ed-26, SC-13, pp. 339-344, June 1978.

R. A. Cliff and T. R. N. Rao, "Improving the Yield of LSI Memory Chips by the Application of Coding", in Proc. 8th Annual Princeton Conf. Information Science, Sept. 1974, pp.386-390.

J. J. Stiffer, "Fault-Tolerant Computing: An Introduction", IEEE Trans. on Computers, vol. C-29, No. 6, June 1980, pp. 417-418.

Bibliography cont.


W. Carter, et al., "Cost Effectiveness of Self Checking Computer Design", in Proceeding International Conference, F. T. C., June 1977.

D. Siewiorek and R. D. Rennels, "Fault-Tolerant VLSI Design", IEEE Computer Journal, pp. 51-53, December 1980.

W. N. Carr and J. B. Mize, MOS/LSI Design and Applications, McGraw Hill Book Co., 1922.

M. Fogiel, Modern Microelectronics, Research and Education Association, New York, 1972.

A. B. Glaser and G. E. Subak-Sharpe, Integrated Circuit Engineering: Design, Fabrication and Applications, Addison-Wesley Publishing Co., Reading, MA, 1977.

"Reliability of Semiconductor Devices", IEEE Proceedings, February 1974.

"Fault-Tolerant Digital Systems", of IEEE Proceedings, February 1974.

G. Moore, "VLSI, Some Fundamental Challenges", IEEE Spectrum, April 1979.

Digest of Papers 1971 International Symposium on Fault-Tolerant Computing, Pasadena, CA, IEEE Computer Society, March 1971.

Digest of Papers 1972 International Symposium on Fault-Tolerant Computing, Newton, MA, IEEE Computer Society, June 1972.

Digest of Papers 1973 International Symposium on Fault-Tolerant Computing, Palo Alto, CA, IEEE Computer Society, June 1973.

Digest of Papers 1974 International Symposium on Fault-Tolerant Computing, Urbana, Ill., IEEE Computer Society, June 1974.

Digest of Papers 1975 International Symposium on Fault-Tolerant Computing, Paris, France, IEEE Computer Society, June 1975

Special Issue on Fault-Tolerant Computing, IEEE Trans. on Computers, vol. C-25, June 1976.

Special Issue on Fault-Tolerant Computing, IEEE Trans. on Computers, vol. C-27, June 1978.